IN THE CLAIMS:

Please amend Claims 1, 3, 5 to 9, 11 to 15, 17 to 20, 22, 23, 25, 26, 28 to 31, 33, 34, 36 and 38 and add new Claims 39 to 42 as shown below. Please cancel Claims 2, 10, 16, 24 and 37 without prejudice or disclaimer of subject matter. The claims, as currently pending in the application, read as follows:

1. (Currently Amended) A protocol data unit switching method ~~that implements switching means~~ used for the selective interconnection of a transmitter port and ~~at least one~~ a plurality of receiver ~~port~~ ports selected from among at least two receiver ports by means of at least one internal bus, ~~each of the~~ said protocol data units being constituted by at least one elementary piece of data, wherein the method ~~implements~~ comprises:

[[-]] a synchronization mechanism defining time slots, ~~known as~~ called connection cycles, on at least one of said internal buses;

[[-]] a mechanism for the allocation of at least one of said connection cycles to each of the selected receiver ports; and

[[-]] a mechanism for the writing of at least one piece of elementary data in the allocated connection cycle or cycles so as to enable the broadcasting of the protocol data unit ~~elementary data~~ to said selected receiver ports,

wherein said writing mechanism comprises a verification step determining whether all the elementary pieces of data constituting the protocol data unit have been received by each of the selected receiver ports,

and wherein the selected receiver ports are blocked until all of them have received all the elementary pieces of data constituting the protocol data unit.

2. (Canceled)

3. (Currently Amended) A method according to claim [[2]] 1, wherein said writing mechanism ~~for writing elementary data in each of the allocated connection cycles~~ is reiterated for any not-yet-serviced selected receiver port, so long as all the elementary pieces of data constituting the protocol data unit have ~~the piece of elementary data has~~ not been received by said not-yet serviced selected receiver port ~~all the receiver ports~~.

4. (Previously Presented) A method according to claim 1, wherein said allocation mechanism comprises a step of association of each of said connection cycles to each of said selected receiver ports.

5. (Currently Amended) A method according to claim 1, wherein said allocation mechanism comprises:

[[-]] a step for the detection of a transmitter port requesting the transfer of at least one protocol data unit towards at least one selected receiver port;

[[-]] a step for verifying that the selected receiver port or ports are ready to receive the protocol data unit or units; and

[[-]] a step for the validation of at least one connection cycle used for the writing of the elementary data of the protocol data unit or units in the selected receiver ports during the validated connection cycle or cycles when the verification is positive.

6. (Currently Amended) A method according to claim 1, ~~implementing~~ further comprising

at least one first input bus multiplexing the elementary pieces of data coming from at least two ~~transmitter~~ ports among said receiver ports and transmitter ports ~~and or~~ and/or

at least one first output bus multiplexing ~~said~~ the elementary pieces of data ~~addressed to~~ coming from at least two ~~receiver~~ ports among said receiver ports and transmitter ports.

7. (Currently Amended) A method according to claim 1, wherein said transmitter and receiver ports are organized in pairs each combining a transmitter port and a receiver port, each pair being associated with a distinct link.

8. (Currently Amended) A method according to claim 1, ~~implementing~~ further comprising at least one link connected to transmitter ports and/or to receiver ports.

9. (Currently Amended) [[An]] A method according to claim 8, wherein the link belongs to the group comprising:

[[-]] ~~the~~ IEEE 1355 or equivalent links; and

[[-]] ~~the~~ external buses.

10. (Canceled)

11. (Currently Amended) A method according to claim 1, wherein said writing mechanism comprises at least one step for the writing of each piece of elementary

data of each of said protocol data units, each of said steps for writing each piece of elementary data comprising:

[[-]] a sub-step for the acceptance, by each of said selected receiver ports, of the writing of each piece of elementary data to be transmitted; and

[[-]] a sub-step for the transmission of said each piece of elementary data to be transmitted, to each of said selected receiver ports.

12. (Currently Amended) A method according to claim 11, wherein during said acceptance ~~stage~~ sub-step, the acceptance is conditioned by a degree of filling of a reception memory associated with said selected receiver port, for each of said receiver ports.

13. (Currently Amended) A method according to claim 1, wherein said writing mechanism comprises at least one step of arbitration for at least one bus connecting a set of at least one input port comprising said transmitter port to a set of at least one output port comprising said receiver ports, said arbitration step being carried out by a switching matrix consisting of crosspoints capable of managing the transmission of ~~transmitting~~ elementary data between an input port and an output port, and being organized in rows and columns,

[[-]] each column (or row respectively) being capable of managing the reception of elementary data coming from an input port associated with the column (or row respectively)[[,]] ; and

[[-]] each row (or column respectively) being capable of managing the transmission of elementary data to an output port associated with the row (or column respectively);

so that a single crosspoint per row (or column respectively), at a given point in time, can enable the transmission of elementary data.

14. (Currently Amended) A method according to claim 1, wherein each protocol data unit transmitted comprises at least one routing header and wherein the method ~~furthermore~~ further comprises:

[[-]] at least one step for the analysis of said routing header; and/or

[[-]] at least one step for the modification of said routing header.

15. (Currently Amended) A protocol data unit switching device ~~implementing switching means to~~ which selectively ~~interconnect~~ interconnects a transmitter port and ~~at least one~~ a plurality of receiver ~~port~~ ports selected from at least two receiver ports by means of at least one internal bus, ~~each of the~~ said protocol data units being ~~formed~~ constituted by at least one piece of elementary data, wherein the device ~~implements~~ comprises:

[[-]] a synchronization ~~means defining~~ unit which defines time slots, ~~known as~~ called connection cycles, [[of]] on at least one of said internal buses;

[[-]] ~~means for allocating~~ an allocation unit which allocates at least one of the connection cycles to each of the selected receiver ports; and

[[-]] ~~means for~~ a writing unit which writes at least one piece of elementary data in the allocated connection cycle or cycles, so as to enable the broadcasting of the protocol data unit ~~said elementary data~~ to the selected receiver ~~ports~~ ports,

wherein said writing unit comprises a verification unit determining whether all the elementary pieces of data constituting the protocol data unit have been received by each of the selected receiver ports,

and wherein the selected receiver ports are blocked until all of them have received all the elementary pieces of data constituting the protocol data unit.

16. (Canceled)

17. (Currently Amended) A device according to claim [[16]] 15, wherein said ~~means for~~ writing unit ~~the elementary data in each of the allocated connection cycles~~ is ~~implemented~~ activated for any not-yet-serviced selected receiver port, so long as all the elementary pieces of data constituting the protocol data unit have ~~the piece of elementary data has~~ not been received by said not-yet-serviced selected receiver port ~~all the receiver ports~~.

18. (Currently Amended) A device according to claim 15, wherein said allocation ~~mechanism comprises a step of associating~~ unit associates each of said connection cycles to each of said selected receiver ports.

19. (Currently Amended) A device according to claim 15, wherein said allocation ~~mechanism comprises~~ unit performs:

[[-]] ~~means for detecting~~ detection of a transmitter port requesting the transfer of at least one protocol data unit towards at least one selected receiver port;

[[-]] ~~means for verifying~~ verification that the selected receiver port or ports are ready to receive the protocol data unit or units; and

[[-]] ~~means for validating~~ validation of at least one connection cycle used for the writing of the elementary data of the protocol data unit or units in the selected receiver ports during[[;]] the validated connection cycle or cycles when the verification is ~~Positive~~ positive.

20. (Currently Amended) A device according to claim 15, further comprising:

~~implementing~~ at least one first input bus multiplexing the elementary pieces of data ~~elements~~ coming from at least two ~~transmitter~~ ports among said receiver ports and transmitter ports, and/or

at least one first output bus multiplexing the ~~pieces of~~ elementary pieces of data ~~addressed to~~ coming from at least two ~~receiver~~ ports among said receiver ports and transmitter ports.

21. (Previously Presented) A device according to claim 15, wherein said transmitter and receiver ports are organized in pairs, each combining a transmitter port and a receiver port, each pair being associated with a distinct link.

22. (Currently Amended) A device according to claim 15, ~~implementing~~ further comprising at least one link connected to transmitter ports and/or to receiver ports.

23. (Currently Amended) A device according to claim 22, wherein the link belongs to the group comprising:

[[-]] ~~the~~ IEEE 1355 or equivalent links; and

[[-]] ~~the~~ external buses.

24. (Canceled)

25. (Currently Amended) A device according to claim 15, wherein said writing ~~means implements a step of writing~~ unit writes each piece of elementary data of each of said protocol data units, and ~~further comprises~~:

[[-]] ~~means for accepting~~ accepts, by each of the selected receiver ports, of the writing of said each piece of elementary data to be transmitted, and

[[-]] ~~means for transmitting of~~ transmits said each piece of elementary data to be transmitted, to each of the selected receiver ports.

26. (Currently Amended) A device according to claim 25, wherein the acceptance implemented by said ~~acceptance means~~ writing unit is conditioned by a degree of filling of a reception memory associated with the selected receiver port, for each of said receiver ports.

27. (Previously Presented) A device according, to claim 26, wherein said memory comprises at least one FIFO.

28. (Currently Amended) A device according to claim 15, wherein said writing ~~means comprises at least one arbitration means of~~ unit arbitrates at least one bus connecting a set of at least one input port comprising said transmitter port to a set of at least one output port comprising said receiver ports, the arbitration step ~~being~~ is carried out by a switching matrix consisting of crosspoints capable of managing the ~~transmitting~~ transmission of elementary data between an input port and an output port, and organized in rows and columns,

[[-]] each said column (or row respectively) being capable of managing the reception of elementary data coming from an input port associated with the column (or row respectively); and

[[-]] each said row (or column respectively) being capable of managing the transmission of elementary data to an output port associated with the row (or column respectively);

so that a single crosspoint per row (or column respectively), at a given point in time, can enable the transmission of pieces of elementary data.

29. (Currently Amended) A device according to claim 15, wherein each protocol data unit transmitted comprises at least one routing header and the ~~method~~ device ~~furthermore~~ further comprises:

[[-]] at least one ~~means~~ unit for the analysis of said routing header; and/or

[[-]] at least one ~~means~~ unit for the modification of said routing header.

30. (Currently Amended) A device according to claim 15, further comprising an interfacing ~~means~~ unit for delivering, to a control module and through clock

signal transmission ~~means~~ unit, clock signals regenerated from packets received by said interfacing ~~means~~ unit.

31. (Currently Amended) A device according to claim 15, further comprising an interfacing ~~means~~ unit for transmitting and/or receiving information through at most two connection buses addressed to and/or coming from at least one of the means belonging to the group comprising said synchronization ~~means~~ unit, said allocation ~~means~~ unit and said writing ~~means~~ unit.

32. (Previously Presented) A device according to claim 31, wherein the protocol data units sent out by at least one emitter port towards FIFOs are multiplexed by a reception linking bus.

33. (Currently Amended) A device according to claim [[15]] 31, wherein the protocol data units received by at least one receiver port through the FIFOs are demultiplexed on a transmission linking bus.

34. (Currently Amended) A switching apparatus comprising:

[[-]] at least one switching device according to claim 15[[,]]; and

[[-]] ~~and~~ [[at.]] at least one element belonging to the group comprising:

[[-]] ~~the~~ IEEE 1355 or equivalent links, and

[[-]] ~~the~~ external buses.

35. (Previously Presented) A switching apparatus according to claim 34, connected to a data processing apparatus.

36. (Currently Amended~~) An application of the~~ A method according to claim 1, wherein the method is applied to at least one of the fields belonging to the group comprising:

[[-]] high bit rate switching;

[[-]] distributed applications;

[[-]] the transmission of digital data;

[[-]] the reception of digital data;

[[-]] audio applications;

[[-]] company networks; and

[[-]] real-time image transmission.

37. (Canceled).

38. (Currently Amended) A computer program stored on a computer-readable medium, ~~product for the switching of~~ the program executing a protocol data unit ~~units implementing~~ switching ~~means~~ method used for the selective interconnection of a transmitter port and ~~at least one~~ a plurality of receiver ~~port~~ ports selected from at least two receiver ports by means of at least one internal bus, ~~each of the~~ said protocol data unit ~~units~~ being constituted by at least one ~~piece of~~ elementary piece of data, the ~~computer~~ program ~~product comprising program code instructions recorded on a carrier that can be used in a computer,~~ comprising:

- ~~programming means readable by computer to carry out~~ a synchronization step defining time slots, ~~known as~~ called connection cycles, on at least one of the internal buses;

- ~~programming means readable by computer to carry out a~~ an allocation step for the allocation of at least one of the connection cycles to each of said selected receiver ports; and

- ~~programming means readable by computer to carry out~~ a writing step for the writing of at least one piece of elementary data in the allocated connection cycle or cycles so as to enable the broadcasting of ~~said elementary data~~ the protocol data unit to said selected receiver ports, said writing step comprising a verification step determining whether all the elementary pieces of data constituting the protocol data unit have been received by each of the selected receiver ports, and the selected receiver ports being blocked until all of them have received all the elementary pieces of data constituting the protocol data unit.

39. (New) A method according to claim 13, wherein at least one column (or row respectively) of said switching matrix comprises at least two crosspoints each associated with a different receiver port, so that at a given point in time a same piece of elementary data can be transferred to the at least two receiver ports associated with said at least two crosspoints.

40. (New) A method according to claim 39, wherein the switching means comprises N receiver ports, and wherein at least one column (or row respectively) of said switching matrix comprises N crosspoints each associated with one of the N receiver ports,

so that at a given point in time a same piece of elementary data can be transferred to the N receiver ports.

41. (New) A device according to claim 28, wherein at least one column (or row respectively) of said switching matrix comprises at least two crosspoints each associated with a different receiver port, so that at a given point in time a same piece of elementary data can be transferred to the at least two receiver ports associated with said at least two crosspoints.

42. (New) A device according to claim 41, wherein the switching means comprises N receiver ports, and wherein at least one column (or row respectively) of said switching matrix comprises N crosspoints each associated with one of the N receiver ports, so that at a given point in time a same piece of elementary data can be transferred to the N receiver ports.